REMARKS

A telephone interview was held with Examiner Patel, in the afternoon of March 22, 2006, by Applicant's representative, Walter Malinowski, to discuss potentially allowable subject matter and avoiding the Background of the Invention at least as an anticipatory reference. Applicant thanks Examiner Patel for his courtesy in granting the interview and in indicating that the amendment of rejected claims 1, 20, and 24 to recite "in a non-testing mode" would overcome the Background of the Invention as an anticipatory reference and that such amendment would be supported by Applicant's disclosure.

Claims 1-4, 6-22, 24, 27, 28, 30, 31, and 34-43 are currently pending. Claims 5, 23, 25, 26, 29, 32, and 33 have been canceled without prejudice. Claims 1, 20, 23, 24, and 31 have been amended to recite "in a non-testing mode" and for clarification purposes. Claims 38-43 have been added. The amendment to claims 1, 20, and 24 is supported by page 8, lines 19-25, page 2, lines 25-38, and elsewhere, of the specification as filed. Claim 31 has been rewritten to incorporate the limitations of indicated-as-allowable claim 33 and intervening claim 32. The support for claims 38-43 is found in page 9, lines 6-8, page 13, lines 13-15, and figures 2A to 2C and elsewhere. It is respectfully submitted that no new matter has been added.

The present invention solves prior art problems with multiple controllers in which "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset of the controllers, or only the defective controller resets and there is insufficient information to solve the defect" (page 2, lines 25-28, of Applicant's specification).

The Patent Office rejected claims 1-4, 6-10, 13-15, 20-21, 24, and 29 under 35 U.S.C. 102(a) as being anticipated by the "Background of the Invention" (BOI).

For a claim to be anticipated by a reference, each and every element of the claim must be disclosed by that reference (MPEP 2131) unless the element is inherent.

Claim 1 recites "A computer program product stored on a computer readable storage medium for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, comprising computer readable program code for performing **in a non-testing mode, the first controller detecting an error in the first controller and thereby initiating a process to maintain data access during failure of the first**

controller, the process to maintain data access during failure of the first controller comprising the first controller instructing the at least one other controller to save the at least one other controller's internal state information; saving internal state information by the first controller; the first controller resetting itself after the saving of its internal state information; pausing operation of the at least one other controller; and the at least one other controller saving internal state information at the time of pausing, in parallel with the first controller's saving of its internal state information; and continuing operation of the at least one other controller, wherein only the first controller resets during the process to maintain data access during failure of the first controller, wherein the first and the at least one other controller make the array of data storage devices appear to a host computer as a single high capacity storage device, wherein the internal state information of the first and the at least one other controller is saved to permit diagnosis of the failure of the first controller."

Claim 20 recites "A method for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, the method comprising **in a non-testing mode, the first controller detecting an error in the first controller and thereby initiating a process to maintain data access during failure of the first controller**, the process to maintain data access during failure of the first controller comprising the first controller saving internal state information; pausing operation of the at least one other controller; and the at least one other controller saving internal state information at the time of pausing without resetting; and, continuing operation of the at least one other controller, wherein only the first controller resets during the process to maintain data access during failure of the first controller, wherein the internal state information of the first and the at least one other controller is saved to permit diagnosis of the failure of the first controller, **wherein one of the first and at least one other controller records the destination of the saved internal state information of an other of the first and at least one other controller**."

Claim 23 has been cancelled without prejudice.

Claim 24 recites "A storage subsystem comprising at least two controllers for managing data storage, the at least two controllers coupled to at least one data storage device, the storage

subsystem further comprising a first controller of the at least two controllers adapted for saving internal state information during a failure of the first controller **in a non-testing mode, the first controller detecting an error in the first controller and thereby initiating a process to maintain data access during failure of the first controller**; and, at least one other controller of the at least two controllers adapted for pausing operation, and continuing operation during the failure of the first controller, wherein only the first controller resets during the process to maintain data access during failure of the first controller, wherein the internal state information of the first and the at least one other controller is saved in order to permit diagnosis of the failure of the first controller."

As noted in the BOI, a problem with the prior art, including that discussed in the BOI, is that the problem is "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset of the controllers, or only the defective controller resets and there is insufficient information to solve the defect." It is during such failures, the BOI teaches that access to the storage devices is prevented or insufficient information is saved so as to solve the defect or error. The BOI neither discloses nor suggests that a first controller's internal state information is saved and at least one other controller's internal state information is saved without resetting the at least one other controller in a non-testing mode. Applicant has amended the language of the claims to more clearly reflect that Applicant's solution is directed to the prior art problem where "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset, or only the defective controller resets and there is insufficient information to solve the defect" (page 2, lines 25-28, of the specification as originally filed) in a non-testing mode.

Regarding the remarks section of page 16 of the Office Action mailed January 4, 2006, Applicant has amended the claims in accordance with page 2, lines 25-28, of the specification as filed, including the incorporation of "in a non-testing mode" in each of claims 1, 20, and 24. It is believed that the amendment to claims 1, 20, and 24 puts these claims into condition for allowance over the Background of the Invention, in particular, and the prior art of record, in general. Accordingly, claims 2-4, 6-19, 21, 22, 27, 28, 30, 38, and 41-43 are allowable over the prior art of record.

Furthermore, claim 20 has been amended to recite "**wherein one of the first and at least**

one other controller records the destination of the saved internal state information of an other of the first and at least one other controller," a limitation believed not to be found in the prior art references. Thus, claim 20 is allowable for this additional reason.

The Patent Office rejected claims 11 and 28 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Fujimoto, U.S. Patent No. 6,477,619. Claim 11 recites "wherein the first controller and the at least one other controller are combined on a single circuit card." Claim 28 recites "wherein at least one of the first controller and the at least one other controller are disposed on a single circuit card." Fujimoto shows a disk controller unit that is made up of what appear to be multiple cards attached to backplane 340 (figure 16). Fujimoto (col. 10, lines 25-63) appear to be silent as to whether a controller is disposed on a single circuit card. Thus, claims 11 and 28 are allowable over the prior art of record for this reason.

Claims 11 and 28 are also allowable because they depend from allowable base claims 1 and 24, respectively.

The Patent Office rejected claims 16, 17, 22, and 30 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness et al., U.S. Patent No. 6,601,138.

Claim 25 has been cancelled without prejudice.

Claims 16, 22, and 30 are allowable because they depend from allowable base claims 1 or 24.

Claim 17 recites "A computer program product as claimed in claim 16, wherein during the at least one other controller pausing operation, saving internal state information at the time of pausing, and continuing operation, interrupts are disabled."

BOI discloses "The feature where a failing controller sends a stop message to other controllers is often disabled in the field because the systems are high availability systems" (page 2, lines 16-18, of Applicant's specification). The feature recited in BOI appears to concern an initial default setting in the system regarding whether to allow the propagation of stop messages and not the disabling of interrupts. Contrary to the assertion by the Patent Office on page 8, last four lines, of the Office Action mailed January 4, 2006, BOI does not appear to disclose or even suggest "interrupts are disabled" as recited in claim 17. A stop message may contain information that other controllers receive through polling rather than by using interrupts. Thus, claim 17 is allowable over the prior art of record for this additional reason.

The Patent Office rejected claim 18 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness, further in view of Skazinski et al., U.S. Patent No. 6,574,790.

Claim 18 recites "A computer program product as claimed in claim 16, wherein a flag is set in a host bus adapter during the saving of internal state information to prevent overlapping saves of internal state information in that adapter."

The Patent Office asserted, in paragraph 5, of the Office Action mailed January 4, 2006, (page 9) "As per claim 18, the combination of BOI and Otterness teaches the claimed invention as described above. However, none of them clearly teach about setting a flag to prevent overlapping saves of internal state information in that adapter. Skazinski teaches that using alternate flag (see line 8, Table 6) which is set to equal to true ("1"), to indicate that an alternate mirror entry 6000 is being used to perform the present mirror cache operation to prevent the problems with respect to mirror operation overlap (e.g., see Col. 22, lines 40-47). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Skazinski's step of setting the flag in the system taught by BOI and Otterness to avoid overlapping saves of internal state information in that adapter."

Skazinski does not disclose setting a flag to prevent overlapping saves of internal state data in that adapter. Skazinski also appears to be concerned with host write data (e.g., column 14, lines 35-48) and not state information, as claimed. Neither Otterness nor the BOI seem to disclose the use of flags. Thus, claim 18 is allowable over the prior art of record for this additional reason.

The Patent Office rejected claims 19 and 23 under 35 U.S.C. 103(a) as being unpatentable over the Background of the Invention in view of Otterness, and further in view of Vishlitzky, U.S. Patent No. 6,047,353.

Claim 23 has been cancelled without prejudice.

Claim 19 is allowable for the reasons claim 1 is allowable.

The Patent Office rejected claims 12, 26, and 27 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Oldfield et al., U.S. Published Patent Applications No. 2002/0133743.

Claim 26 has been cancelled without prejudice.

Claim 27 is allowable because it depends from allowable claim 24.

Claim 12 recites "A computer program product as claimed in claim 1, wherein in addition to the internal state information, at least one of the first controller and the at least one other controller save external memory data corresponding to an interface chip trace area." The limitation of claim 12 is not met by either the BOI or Oldfield; especially since neither the BOI nor Oldfield appear to teach an interface chip trace area. Thus, claim 12 is allowable over the prior art of record for this additional reason.

The Patent Office rejected claims 31, and 34-37 under 35 U.S.C. 103(a) as unpatentable over DeKoning in view of BOI and further in view of Okazaki.

The Patent Office rejected claim 32 under 35 U.S.C. 103(a) as unpatentable over DeKoning in view of BOI and further in view of Okazaki and further in view of Kahle.

For a claim to be anticipated by a reference, each and every element of the claim must be disclosed by that reference (MPEP 2131) unless the element is inherent.

Claim 31 recites "A Fibre Channel Arbitrated Loop storage system comprising a first set of disk drives connected to a first set of loops, and a second set of disk drives redundant with the first set of disk drives and connected to a second set of loops; wherein a first adapter is connected to the first set of loops and a second adapter is connected to the second set of loops; each adapter being adapted for issuing a command to the other adapter to save internal status data and not reset itself, wherein each adapter is adapted for saving internal status data and resetting, wherein a flag is set when internal status data save operation is occurring to prevent another internal status data save operation from being invoked, wherein the flag is set to prevent the another internal status data save operation from being invoked before the greater time period of the group consisting of a set timeout period and the time period to write the internal status data to a memory."

As Applicant has amended claim 31 to incorporate the indicated-as-allowable subject matter of claim 33 and intervening claim 32, Applicant respectfully submits that claims 31 and 34-37 are in condition for allowance.

Applicant believes newly added claims 38-43 are allowable over the prior art of record.

Regarding the remarks section of the Office Action mailed on January 4, 2006. The Patent Office asserted in Paragraph 13 "As to the remark, Applicant asserted: (a) The BOI neither discloses nor suggests that a first controller's internal state information is saved and at least one other controller's internal state information is saved without resetting the at least one other

controller. (b) Neither the BOI nor Okazaki, alone or in combination, disclose or fairly suggest the first an other storage controllers storing their internal state information where only the first storage controller resets. (c) Applicant challenges the taking of Official Notice and requests an appropriate teaching (i.e., a reference) and motivation (e.g., preferably from that reference) be provided for these limitations. (d) BOI does not appear to disclose or even suggest "interrupts are disabled" as recited in claim 17. (e) None of BOI and Otterness clearly teach about setting a flag to prevent overlapping saves of internal state information in that adapter. (f) Skazinski does not disclose setting a flag to prevent overlapping saves of internal state data in that adapter. Skazinski also appears to be concerned with host write data (e.g., column 14, lines 35-48) and not state information, as claimed. (g) Neither Otterness nor the BOI seem to disclose the use of flags. (h) Mason does not disclose or suggest that the host bus adapter saves information relating to an interface chip area. (i) Neither the BOI nor Okazaki, alone or in combination, disclose or fairly suggest the first and other storage controllers storing their internal state information where only the first storage controller resets."

Regarding points a) and b), the present invention solves prior art problems with multiple controllers in which "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset of the controllers, or only the defective controller resets and there is insufficient information to solve the defect" (page 2, lines 25-28, of Applicant's specification). Applicant believes that the claims presented in the last response sufficiently drafted around the prior art recognized by Applicant in the BOI. To facilitate prosecution, Applicant has amended the independent claims to further clarify Applicant's invention. Applicant believes all independent claims (i.e., 1, 20, 24, and 31) clearly describe applicant's invention such that the claimed invention cannot be construed as falling into one of the two prior art techniques applicant has recognized in the BOI. In fact with the incorporation of the limitations of claims 32 and 33 into claim 31, claim 31 and its dependents clearly should be in condition for allowance.

Regarding point c), Fujimoto does not appear to provide a teaching of a single card. A controller is shown by Fujimoto to consist of several cards in a backplane (figure 16).

Regarding point d), a stop message is not an interrupt. Controllers may communicate with each other using a polling method.

Regarding point e), claim 18 recites "wherein a flag is set in a host bus adapter during the

saving of internal state information to prevent overlapping saves of internal state information in that adapter." The Patent Office asserted that Skazinski (Table 6, line 8, and col. 22, lines 40-47) disclose the limitations of Claim 18. Skazinski discloses (col. 1, line 64, through col. 2, line 23) "in the event of a single controller failure, the surviving controller is able to take over the tasks that were being performed by the failed controller, and perform those tasks that were scheduled to be performed by the failed controller. To take over the tasks of a failed controller, a surviving controller must keep track of both the tasks that its partner controller is working on, and the tasks that its partner controller is scheduled to work on before the failure occurs. To illustrate this, consider, for example, that a controller fails before data stored in its cache (in response to a write request from a host computer) is written onto a system drive. Data in the cache of a failed controller is lost unless a battery backup is used. In this situation, it is desirable for a surviving controller to complete the scheduled task of the failed controller by writing the data that was in the failed controller's cache onto the system drive. To accomplish this, a surviving controller in active configuration would need to have a copy, or a mirror of the failed controller's cache. State-of-the-art data storage systems are limited because there are no known structure or procedures for copying or mirroring a controller's cache between other different controllers in active configuration. Therefore, what is needed, is a cache mirroring system, apparatus, and method for multi-controller environments." Skazinski discloses (col. 22, lines 40-47) "Finally, using alternate flag (see line 8, Table 6) is set to equal to true ("1"), to indicate that an alternate mirror entry 6000 is being used to perform the present mirror cache operation to prevent the problems discussed in greater detail above with respect to mirror operation overlap. In this manner, CDMP 300 sets up the mirror operation to mirror to an alternate mirror cache line." Even though Skazinski discloses flags to prevent mirror operation overlap, Skazinski is directed to the mirroring of cache data of an adapter so that the tasks of any controller are not lost and does not disclose the setting of a flag within an adapter "wherein a flag is set in a host bus adapter during the saving of internal state information to prevent overlapping saves of internal state information in that adapter." That is, even though Skazinski discloses flags, the flags of Skazinski prevent mirror data overlaps and are not set within an adapter to prevent overlapping saves of internal state information in that adapter. Thus, claim 18 is not made obvious by the BOI, Otterness, and Skazinski, alone or in combination.

Regarding point h), Applicant encourages the Patent Office to point out what the Patent Office believes to be patentable subject matter.

Regarding point i), the Patent Office did not enter a point i). Applicant notes that the present invention solves prior art problems with multiple controllers in which "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset of the controllers, or only the defective controller resets and there is insufficient information to solve the defect" (page 2, lines 25-28, of Applicant's specification). For clarification purposes, Applicant has amended claims 1, 20, and 24 to recite "in a non-testing mode."

Applicant believes newly added claims 38-43 are allowable over the prior art of record.

The Patent Office is respectfully requested to reconsider and remove the rejections of the claims under 35 U.S.C. 103(a) based on BOI, Otterness, DeKoning, Oldfield, Skazinski, Vishlitzky, Fujimoto, and Okazaki, alone or in combination, and to allow all of the pending claims 1-4, 6-22, 24, 27, 28, 30, 31, and 34-43 as now presented for examination. An early notification of the allowability of claims 1-4, 6-22, 24, 27, 28, 30, 31, and 34-43 is earnestly solicited.

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Respectfully submitted:

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